

CLAIMS

What is claimed is:

1. A delay stage circuit of a ring oscillator for setting a delay value of the delay stage circuit and a corresponding frequency of operation of the ring oscillator, the delay stage circuit comprising:

a differential transistor pair for receiving an input oscillation signal and for producing a corresponding output oscillation signal characterized by a delay, wherein the differential transistor pair is coupled to receive a bias signal set by an external bias circuit;

an active load further comprising a pair of MOSFET devices, each having a drain coupled to a supply, a source coupled to a drain of one device of the differential transistor pair and a gate coupled to a selectable resistive load that is further coupled to the supply; and

wherein the selectable resistive load comprises a plurality of resistive devices that, when coupled in series with a gate-to-source capacitance provided by the pair of MOSFET devices, generates a desired R-C time constant to define the delay of the differential transistor pair.

2. The delay stage circuit of claim 1 wherein the selectable resistive load further includes a plurality of parallel coupled resistors wherein at least one resistor is selectable.

3. The delay stage circuit of claim 2 wherein the at least one selectable resistor is a resistor configured MOSFET.

4. The delay stage circuit of claim 2 wherein the at least one selectable resistor is a traditional resistive element coupled in series with a selectable switch.

5. The delay stage circuit of claim 2 wherein the selectable resistive load further includes a plurality of scaled parallel coupled resistors that, when selected and coupled to the gate-to-source capacitance of a corresponding active load, provide an R-C time constant that generates a corresponding delay.

6. The delay stage circuit of claim 5 wherein the total delay of the delay elements of the ring oscillator results in a frequency of operation of the ring oscillator that is approximately equal to one of 2.5 GHz, 3.125 GHz, 4.0 GHz, and 5.0 GHz.

7. A ring oscillator, comprising:

- a plurality of delay stages coupled serially in a loop, each delay stage further comprising an input for receiving an oscillation signal and an output for producing a corresponding oscillation signal characterized by a delay;

- a bias circuit for selectively providing a bias signal to the plurality of delay stages to adjust the delay of the corresponding output oscillation signal;

- wherein each delay stage further includes:

- a differential transistor pair for receiving an input oscillation signal and for producing a corresponding output oscillation signal characterized by the delay, wherein the differential transistor pair is coupled to receive the bias signal provided by the bias circuit; and

- an active load comprising a pair of MOSFET devices, each having a drain coupled to a supply, a source coupled to a drain of one device of the differential transistor pair and a gate coupled to a selectable resistive load that is further coupled to the supply; and

wherein the selectable resistive load comprises a plurality of resistive devices that, when coupled in series with a gate-to-source capacitance provided by the pair of MOSFET devices, generates a desired R-C time constant to define the delay of the differential transistor pair.

8. The ring oscillator of claim 7 wherein a frequency of oscillation of the ring oscillator is a function of the delay of each delay stage circuit of the ring oscillator as set by the selectable resistive load and as a function of the externally provided bias signal that adjusts a bias level of the differential transistor pair.

9. The ring oscillator of claim 7 wherein the selectable resistive load further includes a plurality of parallel coupled resistors wherein at least one resistor is selectable.

10. The ring oscillator of claim 9 wherein the at least one selectable resistor is a resistor configured MOSFET.

11. The ring oscillator of claim 9 wherein the at least one selectable resistor is a traditional resistive element coupled in series with a selectable switch.

12. The ring oscillator of claim 9 wherein the selectable resistive load further includes a plurality of parallel coupled resistors that, when selected and coupled to the gate-to-source capacitance, provides an R-C time constant that generates a corresponding delay.

13. The ring oscillator of claim 12 wherein the total delay of the delay stages of the ring oscillator results in a frequency of operation of the ring oscillator that is approximately equal to one of 2.5 GHz, 3.125 GHz, 4.0 GHz, and 5.0 GHz.

14. A delay stage circuit of a ring oscillator for setting a delay value of the delay stage and a corresponding frequency of operation of the ring oscillator, the circuit comprising:

- a differential transistor pair for receiving an input oscillation signal and for producing a corresponding output oscillation signal characterized by a delay, the differential transistor pair coupled to receive a bias signal set by an external bias circuit;

- an active load comprising a pair of current mirrors, each current mirror including:

- a MOSFET mirror device each having a source coupled to a supply, a drain coupled to a drain of each device of the differential transistor pair and a gate coupled to a selectable load;

- a current mirror reference device coupled to the gate of the MOSFET device, the current mirror reference device for setting a current level in the MOSFET mirror device; and

- wherein the selectable load coupled to the gate of the MOSFET device comprises a plurality of capacitive devices coupled between the gate of the MOSFET device and the supply, a plurality of resistive devices coupled between the gate of the MOSFET device and the drain of the MOSFET device, and wherein the resistive and capacitive devices generate a desired R-C time constant to define the delay of the differential transistor pair.

15. The delay stage circuit of claim 14 wherein a frequency of oscillation of the ring oscillator is a function of the delay of each delay stage circuit of the ring oscillator as set by the selectable load and as a function of the externally provided bias signal that adjusts a bias level of the differential transistor pair..

16. The delay stage circuit of claim 14 wherein the selectable load further includes at least one selectable resistive device and a corresponding selectable capacitive device.

17. The delay stage circuit of claim 14 wherein the at least one of the plurality of resistive devices is a resistor configured MOSFET.

18. The delay stage circuit of claim 14 wherein the at least one of the plurality of capacitive devices is a capacitor configured MOSFET.

19. The delay stage circuit of claim 14 wherein the at least one of the plurality of resistive devices is a traditional resistive element coupled in series with a selectable switch.

20. The delay stage circuit of claim 14 wherein the at least one of the plurality of capacitive devices is a traditional capacitive element coupled in series with a selectable switch.

21. The delay stage circuit of claim 14 wherein the selectable loads further include a plurality of scaled parallel coupled resistors that, when selected and coupled in series with a plurality of scaled parallel coupled capacitors, provide an R-C time constant that generates a corresponding delay.

22. The delay stage of claim 21 wherein the total delay of the delay stages of the ring oscillator result in a frequency of operation of the ring oscillator that is approximately equal to one of 2.5 GHz, 3.125 GHz, 4.0 GHz, and 5.0 GHz.

23. A programmable multi-gigabit transceiver, comprising:
programmable physical media attachment (PMA) transmit
and receive module for transmitting and receiving high-speed
serial data;

phase-locked loop (PLL) circuitry producing clock
signals for transmit and receive operations of the PMA
transmit and receive module; and

a ring oscillator of the PLL further including a
plurality of delay stages circuits, each of the plurality of
delay stage circuits further including:

a differential transistor pair coupled to receive
an oscillation, the differential transistor pair coupled
to an active load that generates a delay for an output
oscillation of the differential transistor pair; and

wherein the active load further includes at least
one of a selectable resistive and capacitive element.